Electronic Version
Stylesheet Version v1.1.1

LSSD-COMPATIBLE EDGE-TRIGGERED SHIFT REGISTER LATCH

Abstract

A shift register latch (SRL) (300, 304, 400) compatible with performing level sensitive scan design (LSSD) testing with a single scan clock (SCAN CLK) and single scan clock tree (64). The SRL includes a master latch (308, 308', 404), a slave latch (312, 312', 408) and a circuit element (328, 328', 416) connected between the scan clock tree and the master latch. The scan clock generates a clock signal (350, 440) having regularly spaced pulses during the scan phase of the LSSD testing. The circuit element generates a short-pulsed signal (354, 354') based on the scan clock signal for triggering the master latch. This short-pulsed signal compensates for any delay in the clock signal due to the physical length of the signal path from the scan clock to the SRL, thereby preventing scanned data from being flushed through a scan chain of the SRLs of the present invention